

### FEATURES

- Isolated, full-duplex RS-485/RS-422 transceiver
- ±8 kV ESD protection on RS-485 input/output pins
- 16 Mbps data rate
- Complies with ANSI TIA/EIA RS-485-A-1998 and ISO 8482: 1987(E)
- Suitable for 5 V or 3 V operation ( $V_{DD1}$ )
- High common-mode transient immunity: >25 kV/μs
- Receiver has open-circuit, fail-safe design
- 32 nodes on the bus
- Thermal shutdown protection
- Safety and regulatory approvals pending
- UL recognition: 5000 V rms isolation voltage for 1 minute per UL 1577
- VDE certificate of conformity
- DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01
- DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000
- $V_{IORM} = 848 V_{PEAK}$
- Operating temperature range: -40°C to +105°C
- Wide-body, 16-lead SOIC package

### APPLICATIONS

- Isolated RS-485/RS-422 interfaces
- Industrial field networks
- INTERBUS
- Multipoint data transmission systems

### FUNCTIONAL BLOCK DIAGRAM

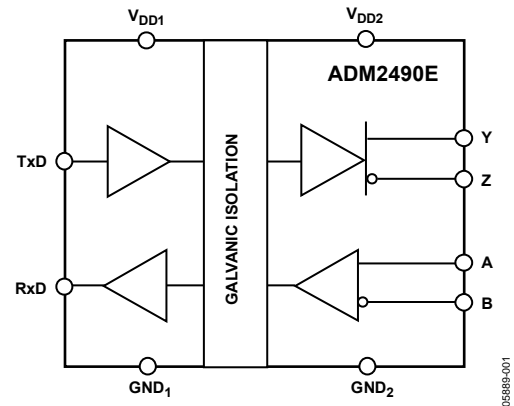


Figure 1.

### GENERAL DESCRIPTION

The ADM2490E is an isolated data transceiver with ±8 kV ESD protection and is suitable for high speed, full-duplex communication on multipoint transmission lines. It is designed for balanced transmission lines and complies with ANSI TIA/EIA RS-485-A-1998 and ISO 8482: 1987(E). The device employs Analog Devices, Inc., *iCoupler* technology to combine a 2-channel isolator, a 3-state differential line driver, and a differential input receiver into a single package.

The differential transmitter outputs and receiver inputs feature electrostatic discharge circuitry that provides protection to ±8 kV using the human body model (HBM). The logic side of the device can be powered with either a 5 V or a 3 V supply, whereas the bus side requires an isolated 5 V supply.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where bus contention could cause excessive power dissipation.

#### Rev. 0

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## REVISION HISTORY

10/06—Revision 0: Initial Version

## SPECIFICATIONS

All voltages are relative to their respective ground;  $2.7 \leq V_{DD1} \leq 5.5 \text{ V}$ ,  $4.5 \text{ V} \leq V_{DD2} \leq 5.5 \text{ V}$ . All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5.0 \text{ V}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>SUPPLY CURRENT</b>						
Power-Supply Current, Logic Side						
TxD/RxD Data Rate < 2 Mbps	$I_{DD1}$			3.0	mA	$2.7 \text{ V} \leq V_{DD1} \leq 5.5 \text{ V}$ , unloaded
TxD/RxD Data Rate = 16 Mbps	$I_{DD1}$			6	mA	100 $\Omega$ load between Y and Z
Power-Supply Current, Bus Side						
TxD/RxD Data Rate < 2 Mbps	$I_{DD2}$			4.0	mA	$2.7 \text{ V} \leq V_{DD1} \leq 5.5 \text{ V}$ , unloaded
TxD/RxD Data Rate = 16 Mbps	$I_{DD2}$			60	mA	100 $\Omega$ load between Y and Z
<b>DRIVER</b>						
Differential Outputs						
Differential Output Voltage, Loaded	$ V_{OD2} $	2.0		5.0	V	$R_L = 50 \Omega$ (RS-422), see Figure 3
		1.5		5.0	V	$R_L = 27 \Omega$ (RS-485), see Figure 3
	$ V_{OD4} $	1.5		5.0	V	$-7 \text{ V} \leq V_{TEST1} \leq +12 \text{ V}$ , see Figure 4
$\Delta V_{OD} $ for Complementary Output States	$\Delta V_{OD} $			0.2	V	$R_L = 54 \Omega$ or 100 $\Omega$ , see Figure 3
Common-Mode Output Voltage	$V_{OC}$			3.0	V	$R_L = 54 \Omega$ or 100 $\Omega$ , see Figure 3
$\Delta V_{OC} $ for Complementary Output States	$\Delta V_{OC} $			0.2	V	$R_L = 54 \Omega$ or 100 $\Omega$ , see Figure 3
Short-Circuit Output Current	$I_{OS}$			200	mA	
Logic Inputs						
Input Threshold Low	$V_{ILTxD}$	$0.25 \times V_{DD1}$			V	
Input Threshold High	$V_{IHTRxD}$			$0.7 \times V_{DD1}$	V	
TxD Input Current	$I_{TxD}$	-10	+0.01	+10	$\mu\text{A}$	
<b>RECEIVER</b>						
Differential Inputs						
Differential Input Threshold Voltage	$V_{TH}$	-0.2		+0.2	V	
Input Voltage Hysteresis	$V_{HYS}$		70		mV	$V_{OC} = 0 \text{ V}$
Input Current (A, B)	$I_I$			1.0	mA	$V_{OC} = 12 \text{ V}$
		-0.8			mA	$V_{OC} = -7 \text{ V}$
Line Input Resistance	$R_{IN}$	12			k $\Omega$	
Logic Outputs						
Output Voltage Low	$V_{OLRxD}$		0.2	0.4	V	$I_{ORxD} = 1.5 \text{ mA}$ , $V_A - V_B = -0.2 \text{ V}$
Output Voltage High	$V_{OHRxD}$	$V_{DD1} - 0.3$	$V_{DD1} - 0.2$		V	$I_{ORxD} = -1.5 \text{ mA}$ , $V_A - V_B = 0.2 \text{ V}$
Short Circuit Current				100	mA	
COMMON-MODE TRANSIENT IMMUNITY <sup>1</sup>		25			kV/ $\mu\text{s}$	$V_{CM} = 1 \text{ kV}$ , transient magnitude = 800 V

<sup>1</sup> CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation.  $V_{CM}$  is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common-mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

# ADM2490E

## TIMING SPECIFICATIONS

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DRIVER</b>						
Maximum Data Rate		16			Mbps	
Propagation Delay	$t_{PLH}, t_{PHL}$		45	60	ns	$R_L = 54\ \Omega, C_{L1} = C_{L2} = 100\ \text{pF}$ , see Figure 6 and Figure 8
Pulse Width Distortion, PWD = $ t_{PYLH} - t_{PYHL} $ , PWD = $ t_{PZLH} - t_{PZHL} $	$t_{PWD}, t_{PWD}$			7	ns	$R_L = 54\ \Omega, C_{L1} = C_{L2} = 100\ \text{pF}$ , see Figure 6 and Figure 8
Single-Ended Output Rise/Fall Times	$t_R, t_F$			20	ns	$R_L = 54\ \Omega, C_{L1} = C_{L2} = 100\ \text{pF}$ , see Figure 6 and Figure 8
<b>RECEIVER</b>						
Propagation Delay	$t_{PLH}, t_{PHL}$			60	ns	$C_L = 15\ \text{pF}$ , see Figure 7 and Figure 9
Pulse Width Distortion, PWD = $ t_{PLH} - t_{PHL} $	$t_{PWD}$			10	ns	$C_L = 15\ \text{pF}$ , see Figure 7 and Figure 9

$T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DRIVER</b>						
Maximum Data Rate		10			Mbps	
Propagation Delay	$t_{PYLH}, t_{PYHL}, t_{PZLH}, t_{PZHL}$		45	60	ns	$R_L = 54\ \Omega, C_{L1} = C_{L2} = 100\ \text{pF}$ , see Figure 6 and Figure 8
Pulse Width Distortion, PWD = $ t_{PYLH} - t_{PYHL} $ , PWD = $ t_{PZLH} - t_{PZHL} $	$t_{PWD}, t_{PWD}$			9	ns	$R_L = 54\ \Omega, C_{L1} = C_{L2} = 100\ \text{pF}$ , see Figure 6 and Figure 8
Single-Ended Output Rise/Fall Time	$t_R, t_F$			27	ns	$R_L = 54\ \Omega, C_{L1} = C_{L2} = 100\ \text{pF}$ , see Figure 6 and Figure 8
<b>RECEIVER</b>						
Propagation Delay	$t_{PLH}, t_{PHL}$			60	ns	$C_L = 15\ \text{pF}$ , see Figure 7 and Figure 9
Pulse Width Distortion, PWD = $ t_{PLH} - t_{PHL} $	$t_{PWD}$			10	ns	$C_L = 15\ \text{pF}$ , see Figure 7 and Figure 9

## ADM2490E CHARACTERISTICS

### PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	
Capacitance (Input-Output) <sup>1</sup>	C <sub>I-O</sub>		3		pF	f = 1 MHz
Input Capacitance <sup>2</sup>	C <sub>i</sub>		4		pF	
Input IC Junction-to-Case Thermal Resistance	θ <sub>JCI</sub>		33		°C/W	Thermocouple located at center of package underside
Output IC Junction-to-Case Thermal Resistance	θ <sub>JCO</sub>		28		°C/W	

<sup>1</sup> Device considered a 2-terminal device: Pins 1, 2, 3, 4, 5, 6, 7, and 8 are shorted together and Pins 9, 10, 11, 12, 13, 14, 15, and 16 are shorted together.

<sup>2</sup> Input capacitance is from any input data pin to ground.

### REGULATORY INFORMATION (PENDING)

Table 5.

UL	VDE
To be recognized under 1577 component recognition program: <sup>1</sup> 5000 V rms isolation voltage	To be certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01: <sup>2</sup> Basic insulation, 848 V peak Complies with DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01, DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000, reinforced insulation, 560 V peak

<sup>1</sup> In accordance with UL1577, each ADM2490E is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 μA).

<sup>2</sup> In accordance with DIN EN 60747-5-2, each ADM2490E is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC).

### INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration.
Minimum External Air Gap (Clearance)	L(I01)	7.45	mm min	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	8.1	mm min	Measured from input terminals to output terminals, shortest distance along body.
Minimum Internal Gap (Internal Clearance)		0.017	mm min	Insulation distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIla		Material Group (DIN VDE 0110, 1/89).

# ADM2490E

## VDE 0884 INSULATION CHARACTERISTICS (PENDING)

This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

An asterisk (\*) on a package denotes VDE 0884 approval for 848 V peak working voltage.

**Table 7.**

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 for Rated Mains Voltage		I to IV	
≤300 V rms		I to II	
≤450 V rms		I to II	
≤600 V rms		40/105/21	
Climatic Classification		2	
Pollution Degree (DIN VDE 0110, see Table 1)		848	V <sub>PEAK</sub>
Maximum Working Insulation Voltage	V <sub>IORM</sub>	1590	V <sub>PEAK</sub>
Input-to-Output Test Voltage, Method b1 V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Tested, t <sub>m</sub> = 1 sec, Partial Discharge < 5 pC	V <sub>PR</sub>		
Input-to-Output Test Voltage, Method a (After Environmental Tests, Subgroup 1) V <sub>IORM</sub> × 1.6 = V <sub>PR</sub> , t <sub>m</sub> = 60 sec, Partial Discharge < 5 pC		1357	V <sub>PEAK</sub>
(After Input and/or Safety Test, Subgroup 2/3) V <sub>IORM</sub> × 1.2 = V <sub>PR</sub> , t <sub>m</sub> = 60 sec, Partial Discharge < 5 pC	V <sub>PR</sub>	1018	V <sub>PEAK</sub>
Highest Allowable Overvoltage (Transient Overvoltage, t <sub>TR</sub> = 10 sec)	V <sub>TR</sub>	6000	V <sub>PEAK</sub>
Safety-Limiting Values (Maximum Value Allowed in the Event of a Failure; see Figure 16)			
Case Temperature	TS	150	°C
Input Current	I <sub>S, INPUT</sub>	265	mA
Output Current	I <sub>S, OUTPUT</sub>	335	mA
Insulation Resistance at T <sub>S</sub> , V <sub>IO</sub> = 500 V	R <sub>S</sub>	>10 <sup>9</sup>	Ω

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted. Each voltage is relative to its respective ground.

**Table 8.**

Parameter	Rating
Storage Temperature	$-55^\circ\text{C}$ to $+150^\circ\text{C}$
Ambient Operating Temperature	$-40^\circ\text{C}$ to $+105^\circ\text{C}$
$V_{DD1}$	$-0.5\text{ V}$ to $+7\text{ V}$
$V_{DD2}$	$-0.5\text{ V}$ to $+6\text{ V}$
Logic Input Voltages	$-0.5\text{ V}$ to $V_{DD1} + 0.5\text{ V}$
Bus Terminal Voltages	$-9\text{ V}$ to $+14\text{ V}$
Logic Output Voltages	$-0.5\text{ V}$ to $V_{DD1} + 0.5\text{ V}$
Average Output Current, per Pin	$\pm 35\text{ mA}$
ESD (Human Body Model) on A, B, Y, and Z pins	$\pm 8\text{ kV}$
$\theta_{JA}$ Thermal Impedance	$73^\circ\text{C/W}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADM2490E

## PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

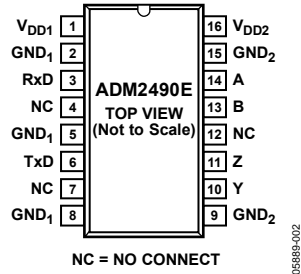


Figure 2. ADM2490E Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Power Supply (logic side). Decoupling capacitor to GND <sub>1</sub> required; capacitor value should be between 0.01 $\mu$ F and 0.1 $\mu$ F.
2, 5, 8	GND <sub>1</sub>	Ground (logic side).
3	RxD	Receiver Output.
4, 7, 12	NC	No Connect. These pins must be left floating.
6	TxD	Transmit Data.
9, 15	GND <sub>2</sub>	Ground (bus side).
16	V <sub>DD2</sub>	Power Supply (bus side). Decoupling capacitor to GND <sub>2</sub> required; capacitor value should be between 0.01 $\mu$ F and 0.1 $\mu$ F.
11	Z	Driver Inverting Output.
10	Y	Driver Noninverting Output.
13	B	Receiver Inverting Input.
14	A	Receiver Noninverting Input.



TEST CIRCUITS

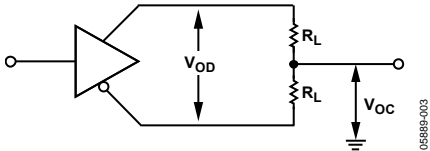


Figure 3. Driver Voltage Measurement

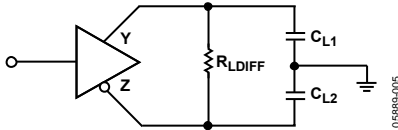


Figure 6. Driver Propagation Delay

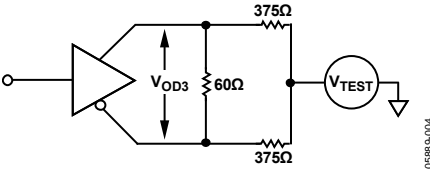


Figure 4. Driver Voltage Measurement

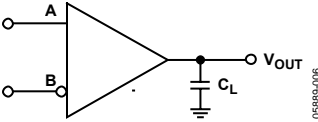


Figure 7. Receiver Propagation Delay

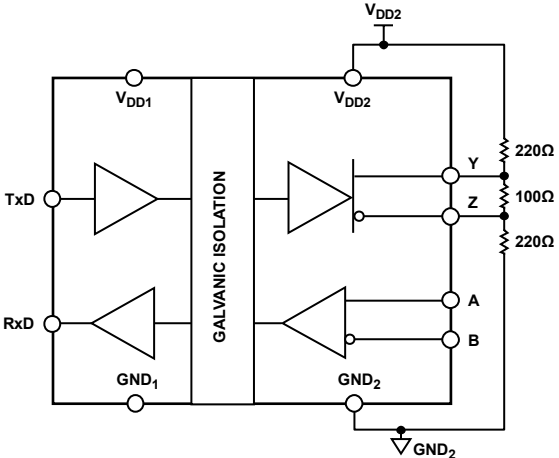


Figure 5. Supply-Current Measurement Test Circuit, See Figure 10 and Figure 11

SWITCHING CHARACTERISTICS

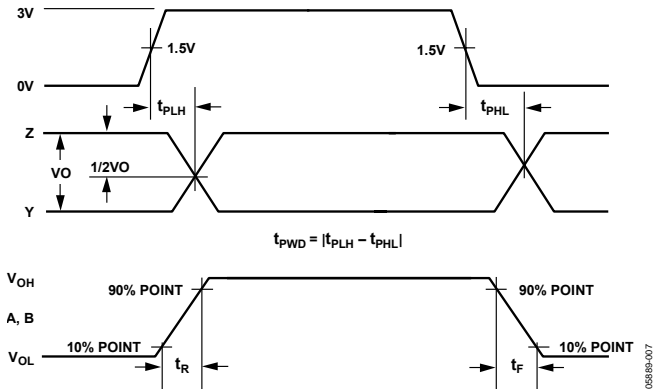


Figure 8. Driver Propagation Delay, Rise/Fall Timing

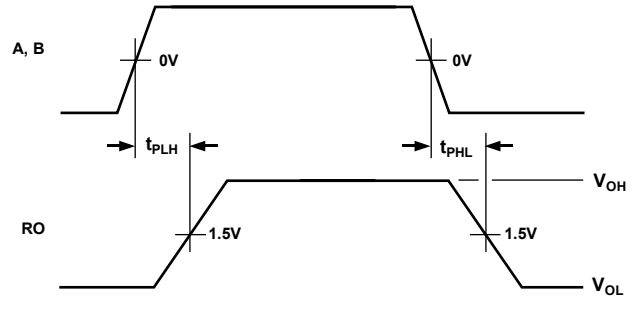


Figure 9. Receiver Propagation Delay

TYPICAL PERFORMANCE CHARACTERISTICS

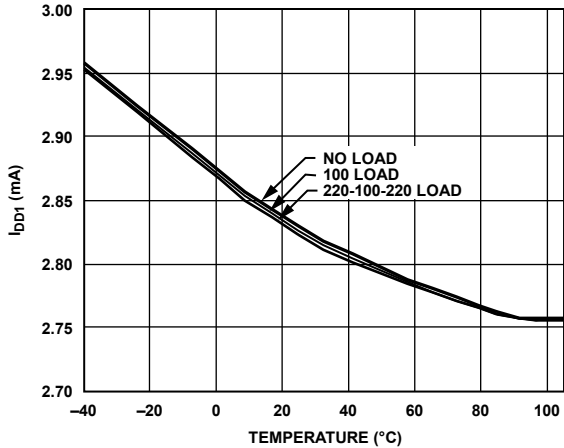


Figure 10.  $I_{DD1}$  Supply Current vs. Temperature (See Figure 5)

05889-015

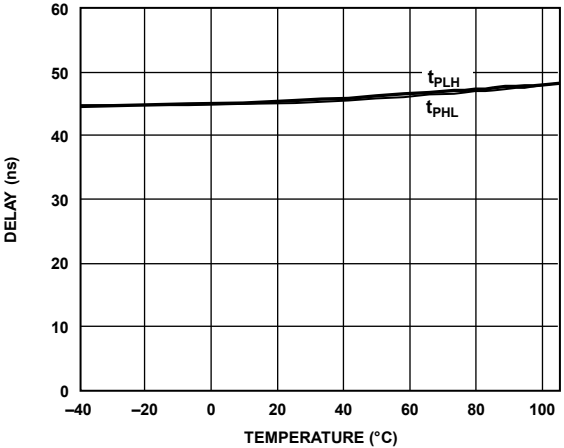


Figure 13. Receiver Propagation Delay vs. Temperature

05889-018

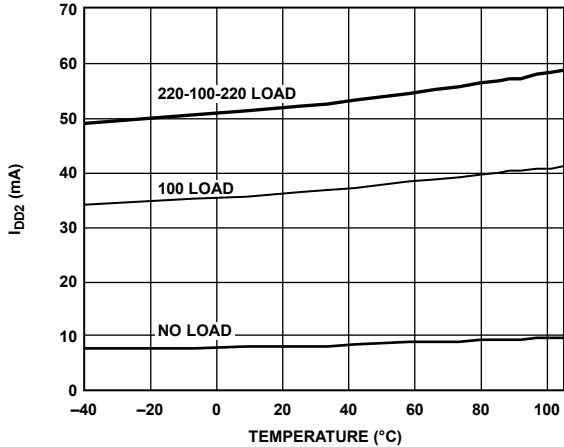


Figure 11.  $I_{DD2}$  Supply Current vs. Temperature (See Figure 5)

05889-016

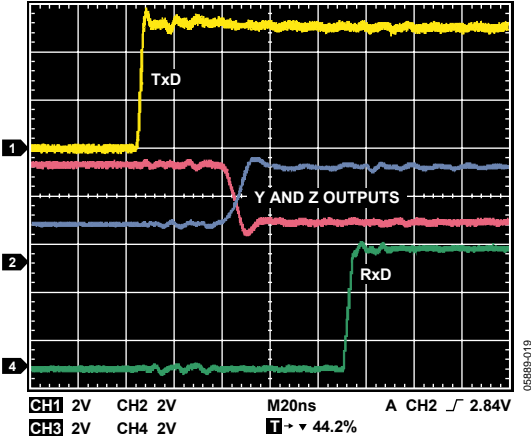


Figure 14. Driver/Receiver Propagation Delay, Low to High ( $R_{LDIFF} = 54 \Omega, C_{L1} = C_{L2} = 100 \text{ pF}$ )

05889-019

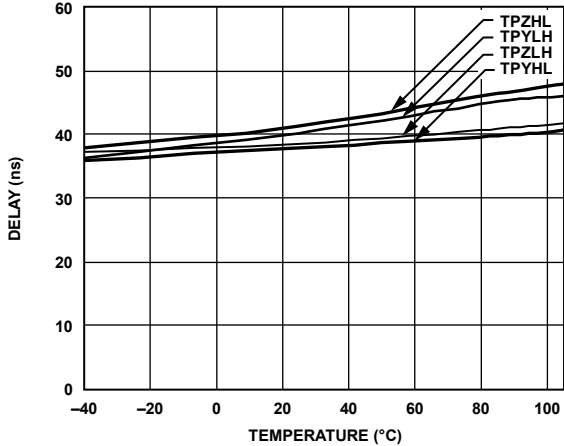


Figure 12. Driver Propagation Delay vs. Temperature

05889-017

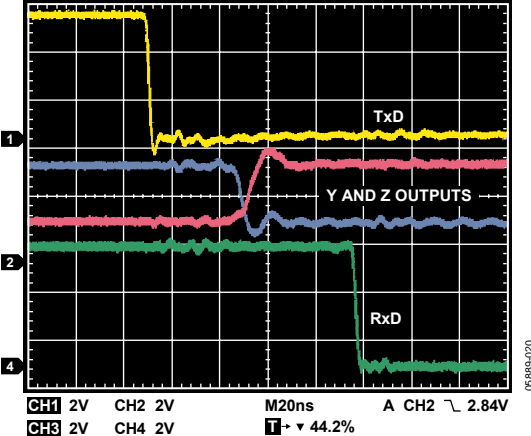


Figure 15. Driver/Receiver Propagation Delay, High to Low ( $R_{LDIFF} = 54 \Omega, C_{L1} = C_{L2} = 100 \text{ pF}$ )

05889-020

# ADM2490E

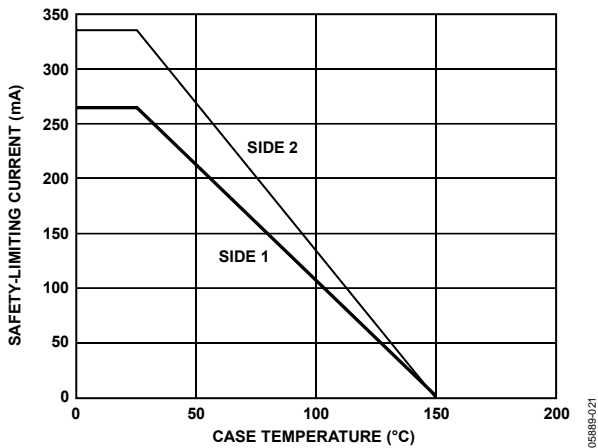


Figure 16. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per VDE 0884

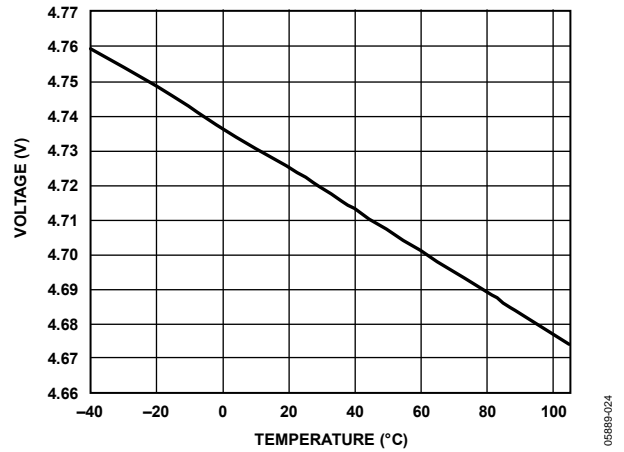


Figure 19. Receiver Output High Voltage vs. Temperature,  $I_{RxD} = -4 \text{ mA}$

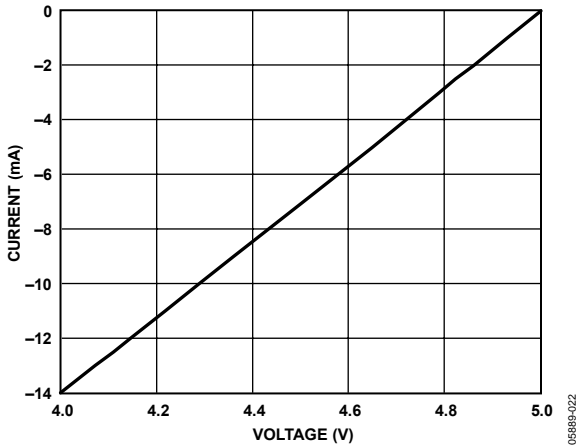


Figure 17. Output Current vs. Receiver Output High Voltage

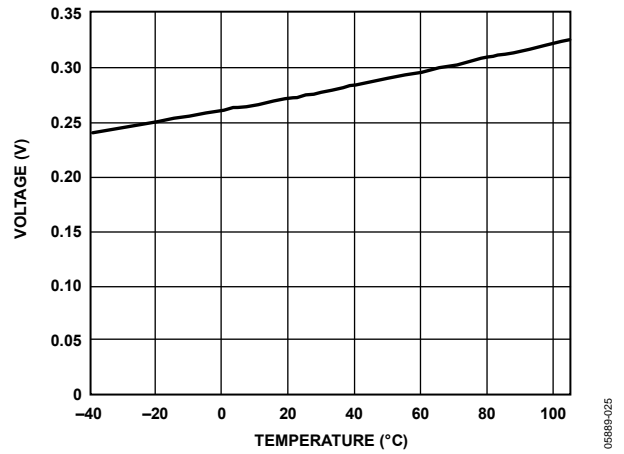


Figure 20. Receiver Output Low Voltage vs. Temperature,  $I_{RxD} = -4 \text{ mA}$

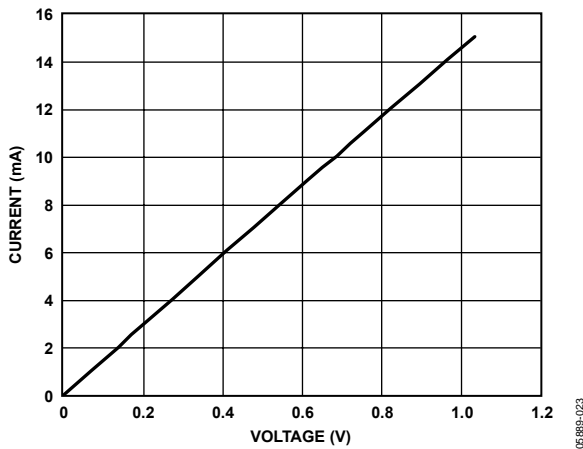


Figure 18. Output Current vs. Receiver Output Low Voltage

## CIRCUIT DESCRIPTION

### ELECTRICAL ISOLATION

In the ADM2490E, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 21). The driver input signal, which is applied to the TxD pin and referenced to logic ground (GND<sub>1</sub>), is coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND<sub>2</sub>). Similarly, the receiver input, which is referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground.

### iCoupler Technology

The digital signals are transmitted across the isolation barrier using iCoupler technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

### TRUTH TABLES

The truth tables in this section use the abbreviations shown in Table 10.

Table 10. Truth Table Abbreviations

Abbreviation	Description
H	High level
I	Indeterminate
L	Low level
X	Irrelevant

Table 11. Transmitting

Supply Status		Input	Outputs	
V <sub>DD1</sub>	V <sub>DD2</sub>	TxD	Y	Z
On	On	H	H	L
On	On	L	L	H

Table 12. Receiving

Supply Status		Inputs	Output
V <sub>DD1</sub>	V <sub>DD2</sub>	A – B (V)	RxD
On	On	>0.2	H
On	On	<-0.2	L
On	On	-0.2 < A – B < +0.2	I
On	On	Inputs open	H
On	Off	X	H
Off	On	X	H
Off	Off	X	L

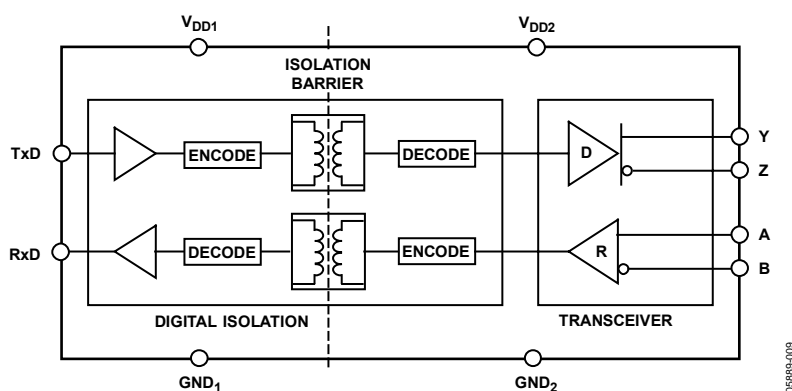


Figure 21. ADM2490E Digital Isolation and Transceiver Sections

# ADM2490E

## THERMAL SHUTDOWN

The ADM2490E contains thermal-shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

## FAIL-SAFE RECEIVER INPUTS

The receiver inputs include a fail-safe feature that guarantees a logic high on the RxD pin when the A and B inputs are floating or open-circuited.

## MAGNETIC FIELD IMMUNITY

Because *i*Couplers use a coreless technology, no magnetic components are present and the problem of magnetic saturation of the core material does not exist. Therefore, *i*Couplers have essentially infinite dc field immunity. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADM2490E is examined because it represents the most susceptible mode of operation.

The limitation on the ac magnetic field immunity of the *i*Coupler is set by the condition that induced an error voltage in the receiving coil (the bottom coil in this case) that was large to either falsely set or reset the decoder. The voltage induced across the bottom coil is given by

$$V = \left( \frac{-d\beta}{dt} \right) \sum \pi r_n^2 ; n = 1, 2, \dots, N$$

where, if the pulses at the transformer output are greater than 1.0 V in amplitude:

$\beta$  = magnetic flux density (gauss).

$N$  = number of turns in receiving coil.

$r_n$  = radius of  $n^{\text{th}}$  turn in receiving coil (cm).

The decoder has a sensing threshold of about 0.5 V; therefore, there is a 0.5 V margin in which induced voltages can be tolerated.

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 22.

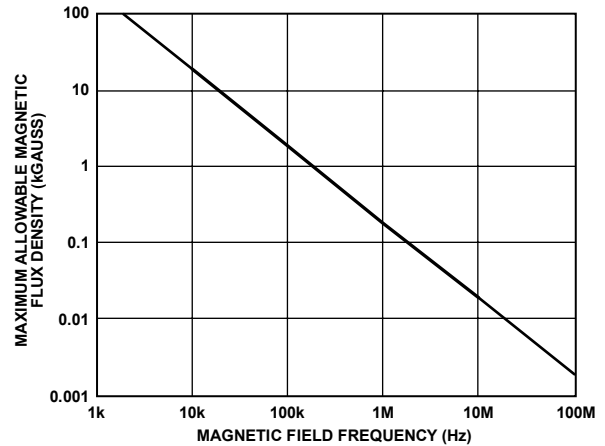


Figure 22. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kGauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

Figure 23 shows the magnetic flux density values in terms of more familiar quantities, such as maximum allowable current flow, at given distances away from the ADM2490E transformers.

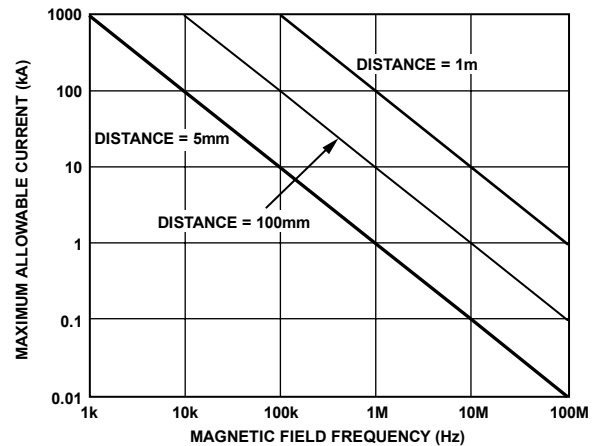


Figure 23. Maximum Allowable Current for Various Current-to-ADM2490E Spacings

With combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

## APPLICATIONS INFORMATION

### ISOLATED POWER-SUPPLY CIRCUIT

The ADM2490E requires isolated power capable of 5 V at up to approximately 75 mA (this current is dependant on the data rate and termination resistors used) to be supplied between the  $V_{DD2}$  and the  $GND_2$  pins. A transformer-driver circuit with a center-tapped transformer and LDO can be used to generate the isolated 5 V supply, as shown in Figure 25. The center-tapped transformer provides electrical isolation of the 5 V power supply. The primary winding of the transformer is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP667 linear voltage regulator provides a regulated power supply to the bus-side circuitry ( $V_{DD2}$ ) of the ADM2490E.

### PC BOARD LAYOUT

The ADM2490E isolated RS-485 transceiver requires no external interface circuitry for the logic interfaces. Power-supply bypassing is required at the input and output supply pins (Figure 24). Bypass capacitors are conveniently connected between Pins 1 and 2 for  $V_{DD1}$  and between Pins 15 and 16 for

$V_{DD2}$ . The capacitor value should be between 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$ . The total lead length between both ends of the capacitor and the input power-supply pin should not exceed 20 mm. Bypassing between Pins 1 and 8 and between Pins 9 and 16 should also be considered unless the ground pair on each package side is connected close to the package.

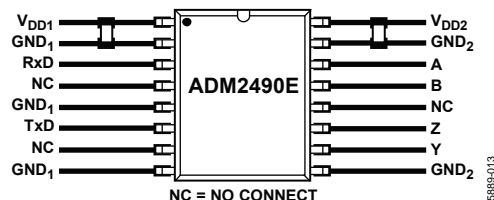


Figure 24. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

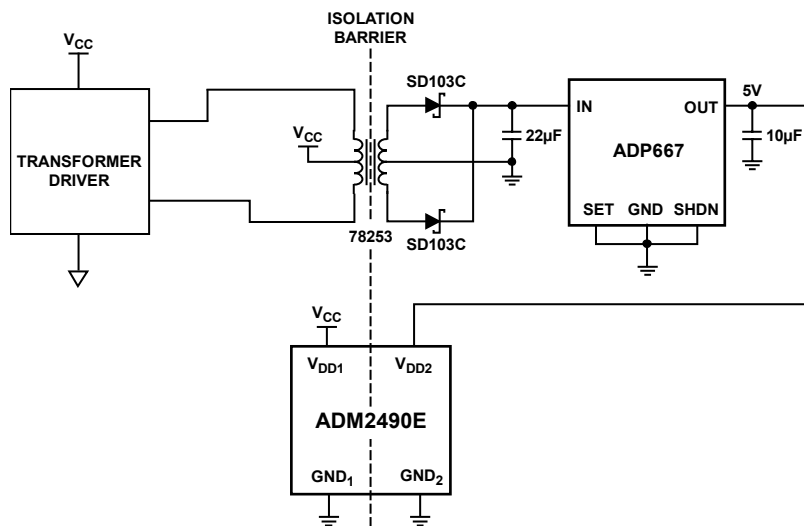
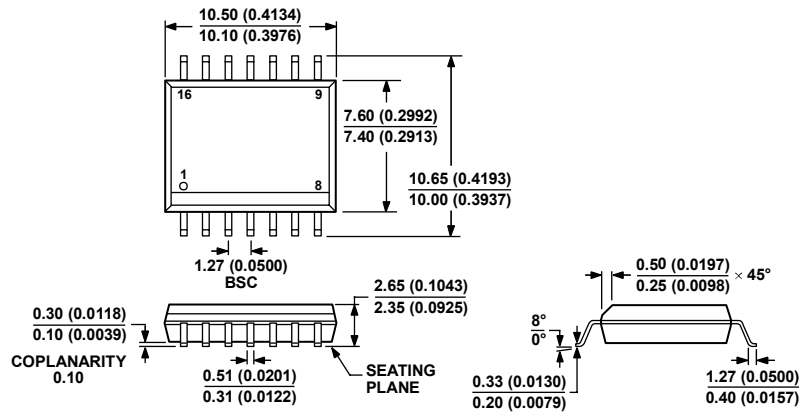


Figure 25. Isolated Power-Supply Circuit

# ADM2490E

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 26. 16-Lead Standard Small Outline Package [SOIC\_W]  
 Wide Body  
 (RW-16)

Dimensions shown in millimeters and (inches)

066806-A

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM2490EBRWZ <sup>1</sup>	-40°C to +105°C	16-Lead Wide Body SOIC_W	RW-16
ADM2490EBRWZ-REEL7 <sup>1</sup>	-40°C to +105°C	16-Lead Wide Body SOIC_W	RW-16

<sup>1</sup> Z = Pb-free part.